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Title: **JP61005295A2: CONTRAST SIGNAL GENERATION CIRCUIT**

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Kind: **A2** Document Laid open to Public inspection (See also: JP07060300B4)

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INPADOC Legal Status: None **Get Now:** Family Legal Status Report

Family:

PDF	Publication	Pub. Date	Filed	Title
☑	**JP61005295A2**	1986-01-11	1984-06-19	CONTRAST SIGNAL GENERATION CIRCUIT
☑	JP07060300B4	1995-06-28	1984-06-19	
2 family members shown above				

Forward References: **Go to Result Set:** Forward references (1)

PDF	Patent	Pub.Date	Inventor	Assignee	Title
☐	US7002537	2006-02-21	Ito; Akihiko	Seiko Epson Corporation	Method of driving electrooptic device, driving circuit, electrooptic device, an electronic apparatus

Other Abstract Info: None

Family list
3 family member for:
JP61005295
Derived from 1 application.

Back to JP61005295

1 **CONTRAST SIGNAL GENERATION CIRCUIT**
Publication info: **JP2022469C C** - 1996-02-26
JP7060300B B - 1995-06-28
JP61005295 A - 1986-01-11

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1. JP,07-060300,B(1995)

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CLAIMS

[Claim(s)]
[Claim 1] A gradation signal creation means create the gradation signal as which gradation is determined with the ratio of ON period and an OFF period in the gradation signal generating circuit for driving a liquid crystal panel by the two or more floor tone, and the above-mentioned ON period and an OFF period are a gradation signal generating circuit characterized by to provide a setting means establish the period for adjustment independently and set up the ratio of ON period within this period for adjustment, and an OFF period.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[Field of the Invention]
This invention relates to the gradation signal generating circuit for carrying out the gradation drive of the liquid crystal panel.
[Description of the Prior Art]
In recent years, the liquid crystal television set which used the liquid crystal display panel for the display is put in practical use as a portable small television set. Moreover, by recently, liquid crystal color television which used the electrochromatic display panel is considered. Although various approaches are shown in an electrochromatic display display, as shown in Fig. 3 , what arranges the primary color filter 1 of R (red), G (green), and B (blue) to a signal electrode, constitutes the electrochromatic display panel 2, and was made to perform color display with the above-mentioned combination in three primary colors is common. Moreover, in Fig. 3 of the above, 3 is a scan electrode drive circuit and n scan signal lines are connected to the electrochromatic display panel 2. Furthermore, as for R signal-electrode drive circuit and 5, 4 is [G signal-electrode drive circuit and 6] B signal-electrode drive circuits, and m signal lines are respectively connected to the electrochromatic display panel 2. 7 [moreover,] -- a liquid crystal electrical-potential-difference generating circuit -- it is -- V0-V5, i.e., V0=GND, and V1= (1/a) -- V5, V2=(2/a) V5, V3=(1-2/a) V5, and V4=(1-1/a) V -- 5 and 5 are generated and each above-mentioned drive circuits 3, 4, 5, and 6 are supplied as operating voltage. In addition, Above a is a bias ratio.
Each signal-electrode drive circuits 4, 5, and 6 in Fig. 3 of the above are constituted as shown in Fig. 4 . That is, each signal-electrode drive circuits 4, 5, and 6 consist of m steps of drive circuits 101-10m. And the 4-bit digital data D1-D4 sent from an image processing circuit (not shown) are first inputted into the register 11 in the drive circuit 101 of the first rank. This register 11 is sent out to the drive circuit 102 of the next step while it inputs the above-mentioned data D1-D4 into read in and a latch circuit 12 synchronizing with sampling clock phiS. The above-mentioned latch circuit 12 latches the data written in the register 11 synchronizing with latch pulse phil, and inputs them into OR circuits 141-144 through inverters 131-134. Moreover, the outputs Q1-Q4 of four bit counters 15 prepared outside are inputted into these OR circuits 141-144. The above-mentioned counter 15 is reset by latch pulse phil, and carries out count-up actuation by clock pulse phiC. And the output of above-mentioned OR circuits 141-144 is inputted into the reset terminal R of a flip-flop 17 through AND circuit 16. This flip-flop 17 is set by latch pulse phil, and that output is sent to a multiplexer 18. While frame change-over signal phiF is given, the liquid crystal driver voltage of V0-V5 is given to this multi-PUREKUTA 18 from the above-mentioned liquid crystal electrical-potential-difference generating circuit 7. And the above-mentioned multiplexer 18 outputs the signal-electrode driving signal Y1, i.e., a gradation signal, according to the output signal of a flip-flop 17. Moreover, the drive circuits 102-10m after the 2nd step as well as the above-mentioned drive circuit 101 are constituted, and output the gradation signals Y2-m.
In the above-mentioned configuration, first, the digital data D1-D4 sent from an image processing circuit are inputted into the drive circuit 101 of the first rank, and are read into a register 11 synchronizing with sampling clock phiS. Synchronizing with sampling clock phiS, the sequential shift of the data D1-D4 read into this register 11 is carried out after that at the drive circuits [102-10m] register 11. And a shift of even the register 11 whose above-mentioned data D1-D4 are 10m of drive circuits gives latch pulse phil after that. As shown in Fig. 5 , whenever sampling clock phiS of m shots is outputted, one shot of this latch pulse phil is outputted, and the data currently held in each drive circuits 101-10m at the register 11 are latched to a latch circuit 12.

Moreover, while a counter 15 is reset by coincidence by the above-mentioned latch pulse phil, as shown in Fig. 5 , a flip-flop 17 is set. By setting this flip-flop 17, the output Yi of a multiplexer 18 starts on the level of V5 from the reference level of V3. In this case, in the following frame, the output Yi of a multiplexer 18 falls from the reference level of V2 to V0 level at the time of the set of a flip-flop 17. A deer is carried out, and the above-mentioned counter 15 starts count actuation by clock pulse phiC, after being reset by latch pulse phil. Above-mentioned clock pulse phiC of 14 shots is generated between each latch pulse phi l, as shown in Fig. 5 . And the count outputs Q1-Q4 of the above-mentioned counter 15 are inputted into OR circuits 141-144 with the signal outputted by minding inverter 131-134 from a latch circuit 12, and the output is inputted into AND circuit 16. Therefore, when the output of OR circuits 141-144 becomes oar "1" with count actuation of a counter 15, the output of AND circuit 16 is set to "1", and a flip-flop 17 is reset. The counted value of the counter 15 with which the output of above-mentioned OR circuits 141-144 serves as oar "1" is determined by the latch data of a latch circuit 12, and time amount after a flip-flop 17 is set by that cause until it is reset is controlled. If the above-mentioned flip-flop 17 is reset, the output of a multiplexer 18 will return to reference level. And the actuation described above by giving latch pulse phil after that is repeated. According to the maintenance data of a latch circuit 12, Signal Yi is outputted from a multiplexer 18 as mentioned above, and the display drive of each signal electrode in the electrochromatic display panel 2 is carried out.
Fig. 6 is what showed the example of a wave of a display driving signal, and the scan electrode driving signal Xi with which (a) is outputted from the scan electrode drive circuit 3, the gradation signal Yi with which (b) is outputted from the multiplexer 18 of the signal-electrode drive circuit 10, and (c) are the synthetic waves of the above-mentioned scan electrode driving signal Xi and the gradation signal Yi.
[Problem(s) to be Solved by the Invention]
As mentioned above, since the output wave decided with the input data is acquired, when the filter thickness of R, G, and B differs from a design value, hues will differ in the conventional signal-electrode drive circuit 10. That is, since the above-mentioned filter forms according to the color of R, G, and B in 3 steps, it is very difficult to form in homogeneity, and it produces variation in filter thickness. If a difference is in filter thickness, even if it impresses the same electrical potential difference to an electrode, a difference will appear in the actual value which joins liquid crystal, and display quality will deteriorate.
This invention can display a desired color correctly, even when it is made in view of the above-mentioned point and the filter thickness of R, G, and B is formed unlike the set point, and it aims at offering the gradation signal generating circuit which can hold display quality good.
[The means for solving a technical problem]
In order to solve the above-mentioned technical problem, a gradation signal creation means create the gradation signal as which gradation is determined with the ratio of ON period and an OFF period, and the above-mentioned ON period and an OFF period establish the period for adjustment independently, and this invention carries out having provided a setting means set up the ratio of ON period within this period for adjustment, and an OFF period as the description in them in the gradation signal generating circuit for driving a liquid crystal panel by the two or more floor tone.
[Function]
Thus, in case the gradation signal as which gradation is determined with the ratio of ON period and an OFF period by constituting according to the data for a display of each primary color is created The above-mentioned ON period and an OFF period can establish the period for adjustment independently, and can tune a gradation expression finely by setting up the ratio of ON period within this period for adjustment, and an OFF period, for example, can use it for adjustment of the color balance of each primary color of R, G, and B.
[Example]
With reference to a drawing, one example of this invention is explained below. In the 1st [**] Fig. R> Fig., 20 is a signal-electrode drive circuit and consists of m steps of drive circuits 201-20m. In the drive circuits 101-10m of Fig. 4 , it is only that the timing of the set signal of a flip-flop 17 differs, and since others are the same configurations as the drive circuits 101-10m of Fig. 4 , these drive circuits 201-20m attach the same sign as the 4th drawing 4 Fig., and omit detailed explanation. A deer is carried out and a set signal is given from the flip-flop 22 with which the above-mentioned flip-flop 17 is formed in the exterior of the signal-electrode drive circuit 20. This flip-flop 22 is reset by 23Qcounter 4 output of 4 bits. This counter 23 carries out count-up actuation by clock pulse phiC2 shown in self Q4 output and 2nd drawing 2 Fig. which are given through OR

circuit 24 while being reset by latch pulse phil. Moreover, the 23Qcounter 4 above-mentioned output is inputted into the reset terminal R of a counter 15 through an inverter 25 while it is inputted into the reset terminal R of a flip-flop 22, as described above. This counter 15 carries out count-up actuation by clock pulse phiC1 shown in Fig. 2 . Moreover, the outputs Q1-Q3 of the above-mentioned counter 23 are inputted into OR circuits 26a-26c. And the initialization data A1 and A2 and A3 are inputted into above-mentioned OR circuits 26a-26c through Inverters 27a-26c. The above-mentioned initialization data A1 and A2 and A3 are amendment data for amending change of the hue accompanying the formation error of filter thickness. And the output of above-mentioned OR circuits 26a-26c is inputted into the reset terminal R of a flip-flop 22 through AND circuit 28. Next, actuation of the above-mentioned example is explained. As shown in a 2nd [**] Fig. R> Fig., this invention divides between each latch pulse phi l into 17 equally, and is generating clock pulse phiC1 in other 15 sections except the first two sections, respectively. The first two sections between each above-mentioned latch pulse phi l are the sections for initial adjustments, and a section setup is performed by 23Qcounter 4 output. Therefore, although clock pulse phiC2 for a count of a counter 23 is set to C1 4 times the frequency of clock pulse phi in this example, an output is forbidden to the timing which latch pulse phil generates. First, the digital data D1-D4 which carry out a deer and are sent from an image processing circuit are inputted into the drive circuit 201 of the first rank, and are read into a register 11 synchronizing with sampling clock phiS. Synchronizing with sampling clock phiS, the sequential shift of the data D1-D4 read into this register 11 is carried out after that at the drive circuits [202-20m] register 11. And a shift of even the register 11 whose above-mentioned data D1-D4 are 20m of drive circuits gives latch pulse phil after that. Whenever sampling clock phiS of m shots is outputted, one shot of this latch pulse phil is outputted, and the data currently held in each drive circuits 201-20m at the register 11 are latched to a latch circuit 12. Moreover, a counter 23 is reset by coincidence by the above-mentioned latch pulse phil. If this counter 23 is reset, the output of "0" and an inverter 25 will be set to "1" by that Q4 output, and a counter 15 will be reset. A counter 15 is held at a reset condition until the contents of the counter 23 count up to "8" after this. Carrying out a deer, the above-mentioned counter 23 starts count-up actuation by clock pulse phiC2, and outputs the count outputs Q1-Q3 to OR circuits 26a-26b. Moreover, these OR circuits 26a-26c are reversed with Inverters 27a-27c, and the initialization data A1 and A2 and A3 are inputted into them. Therefore, if it counts up by clock pulse phiC2 after the above-mentioned counter's 23 resetting and the counted value becomes equal to the initialization data A1 and A2 and A3, the output of OR circuits 26a-26c serves as oar "1", from AND circuit 28, "1" signal will be outputted and a flip-flop 22 will be set. Consequently, an output signal wave as shown in Fig. 2 (e) - (g) according to the initialization data A1 and A2 and contents [of A3] "000" - "111" is acquired from a flip-flop 22. Now, the data of "010" are reversed with Inverters 27a-27c, and the thing which set the initialization data A1 and A2 and A3 as "101", then its setting data are inputted into AND circuit 28 through OR circuits 26a-26c. Therefore, if the above-mentioned counter 24 counts clock pulse phiC2 after reset and counts up to "5", the outputs Q1-Q3 will be set to "101", and the initialization data A1 and A2, A3, or an output, i.e., the output of OR circuits 26a-26c, will serve as oar "1." For this reason, the output of AND circuit 28 is set to "1", and sets a flip-flop 22. For this reason, the output of a flip-flop 22 is set to "1", a flip-flop 17 is set, and that output is sent to a multiplexer 18. The gradation signal Yi is outputted from a multiplexer 18 by this, and the display drive of the signal electrode of a display panel is carried out. And if a counter 23 counts up to 8 after that, an output signal Q4 will be set to "1", and will reset a flip-flop 22. Between after a counter 23 is reset by latch pulse phil as mentioned above until Q4 output signal is outputted is the section for initial adjustments, and the period t2 until a flip-flop 22 is reset by 23Qcounter 4 output the period t1 after a flip-flop 22 is reset in this section for initial adjustments until it is set, and after that is ******(ed) by the initialization data A1 and A2 and A3. If a deer is carried out, and Q4 signal is outputted from a counter 23 as described above, the output of an inverter 25 will be set to "0" and the reset condition of a counter 15 will be canceled. For this reason, a counter 15 starts count actuation by clock pulse phiC1 after that. Above-mentioned clock pulse phiC of 15 shots will be generated by the time each following latch pulse phil is outputted after reset discharge, as shown in Fig. 2 . And the count outputs Q1-Q4 of the above-mentioned counter 15 are inputted into OR circuits 141-144 with the signal outputted through inverters 131-134 from a latch circuit 12, and the output is inputted into AND circuit 16. Therefore, when the output of OR circuits 141-144 becomes oar "1" with count actuation of a counter 15, the output of AND circuit 16 is set to "1", and a flip-flop 17 is reset. The counter value of the counter 15 with which the output of above-mentioned OR circuits 141-144 serves as oar "1" is determined by the latch data of a latch circuit 12, and time

amount after a flip-flop 17 is set by that cause until it is reset is controlled. For example, when the data of "8" are latched to a latch circuit 12, as shown in Fig. 2 , when a counter 15 counts eight clock pulse phiC, the output of AND circuit 16 is set to "1", and a flip-flop 17 is reset. The output of a multiplexer 18 returns to reference level by resetting this flip-flop 17. Thus, the period tR when the flip-flop 17 is set according to the maintenance data of a latch circuit 12 and which period-tP(s) and is reset is determined. Fig. 2 (h), (i), (j), and (k) are what showed the output of a flip-flop 17, and when the initialization data A1 and A2 and A3 are set as "101", they are the case where "0001", "0001", "1111", and "1000" are given as input data D1-D4. Moreover, for Fig. 2 (l) - (n), the scan electrode driving signal Xi with which it is what showed the example of a wave of a display driving signal, and (l) is outputted from a scan electrode drive circuit, and (m) are the multiplexer of the signal-electrode drive circuit 20. The gradation signal Yi outputted from 18 and (n) are the synthetic waves of the above-mentioned scan electrode driving signal Xi and the gradation signal Yi.

Since the initialization data A1 and A2 and A3 can adjust the gradation signal Yi to eight steps in two or more steps, for example, the above-mentioned example, in each gradation as mentioned above, even when filter thickness differs from a design value, a hue can be correctly set up by adjusting the initialization data A1 and A2 and A3.

In addition, although the section for adjustment was established in the preceding paragraph of a gradation wave in the above-mentioned example, you may prepare in the latter part of a gradation wave.

[Effect of the Invention]

As a full account was given above, in case the gradation signal as which gradation is determined with the ratio of ON period and an OFF period is created according to the gradation signal generating circuit of this invention The above-mentioned ON period and an OFF period can establish the period for adjustment independently, and can tune a gradation expression finely by setting up the ratio of ON period within this period for adjustment, and an OFF period, for example, can use it for adjustment of the color balance of each primary color of R, G, and B.

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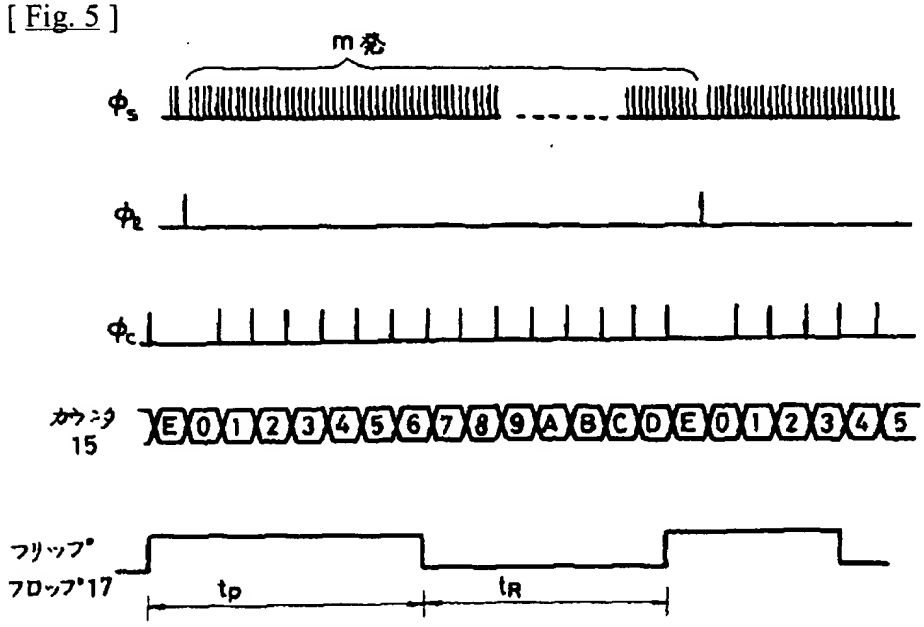
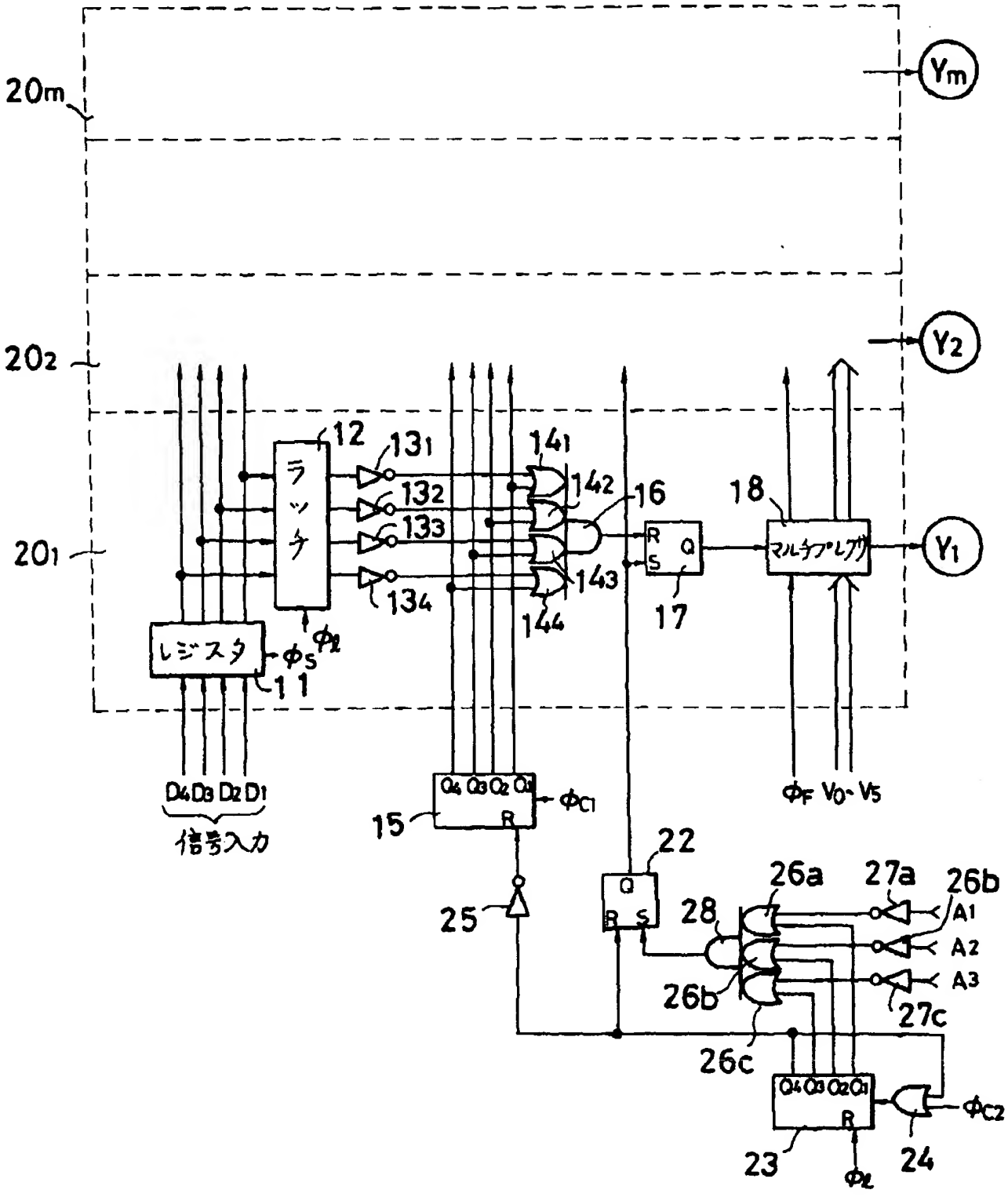
DRAWINGS

[Fig. 5]



[Fig. 1]


20m
Ym
20₂
Y2
20₁
Y1
12
13₁
13₂
13₃
13₄
14₁
14₂
14₃
14₄
16
17
18
ラッチ
レジスタ
11
φS
φL
マルチプレクサ
D4 D3 D2 D1
信号入力
Q4 Q3 Q2 Q1
R
φC1
15
φF V0- V5
22
25
26a
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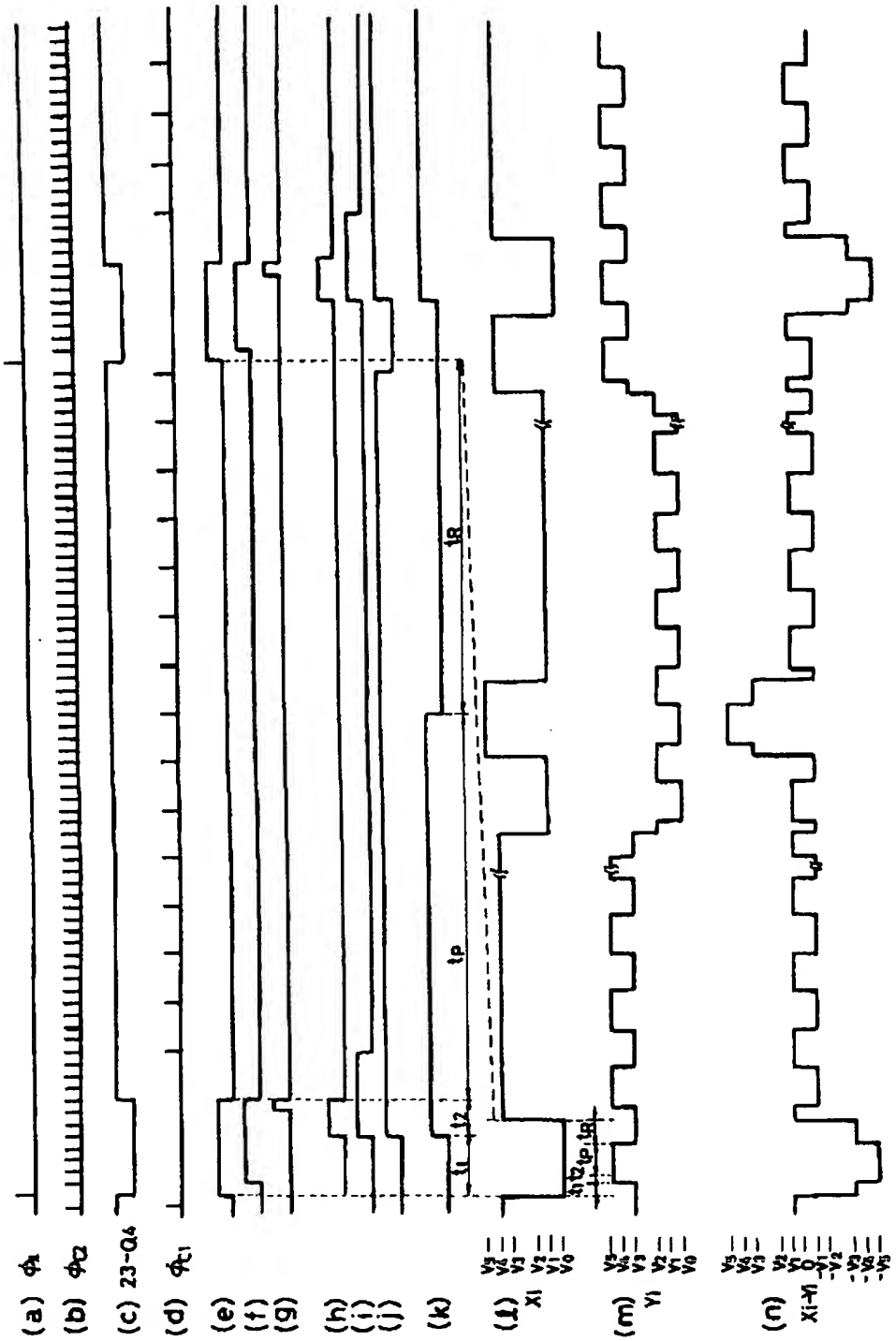
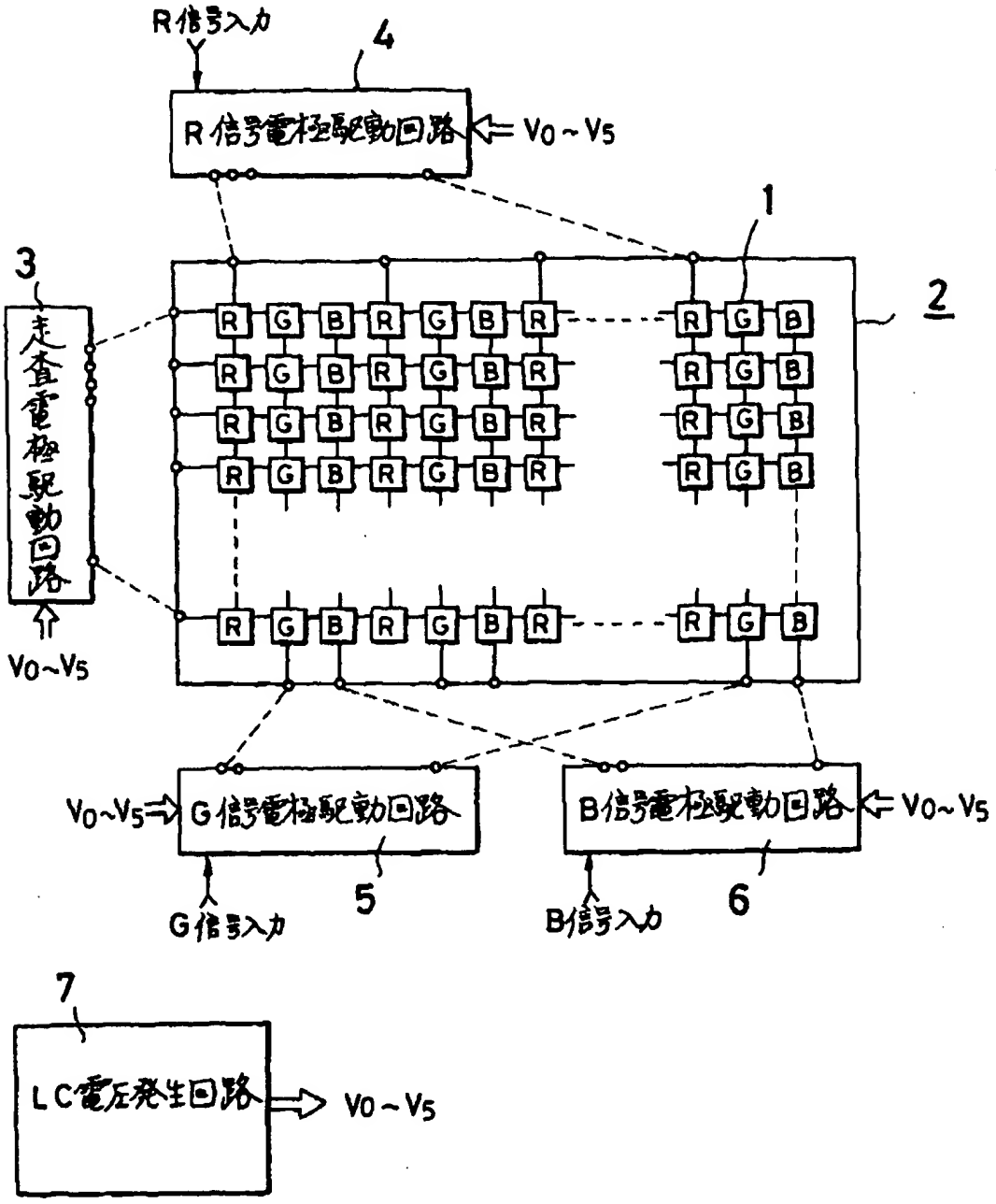
A3
28
26b
27c
26c
φC2
23
24
φL

[Fig. 2]



[Fig. 3]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R信号電極駆動回路
V0~V5
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3
走査電極駆動回路
2
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V0~V5
V0~V5
G信号電極駆動回路
B信号電極駆動回路
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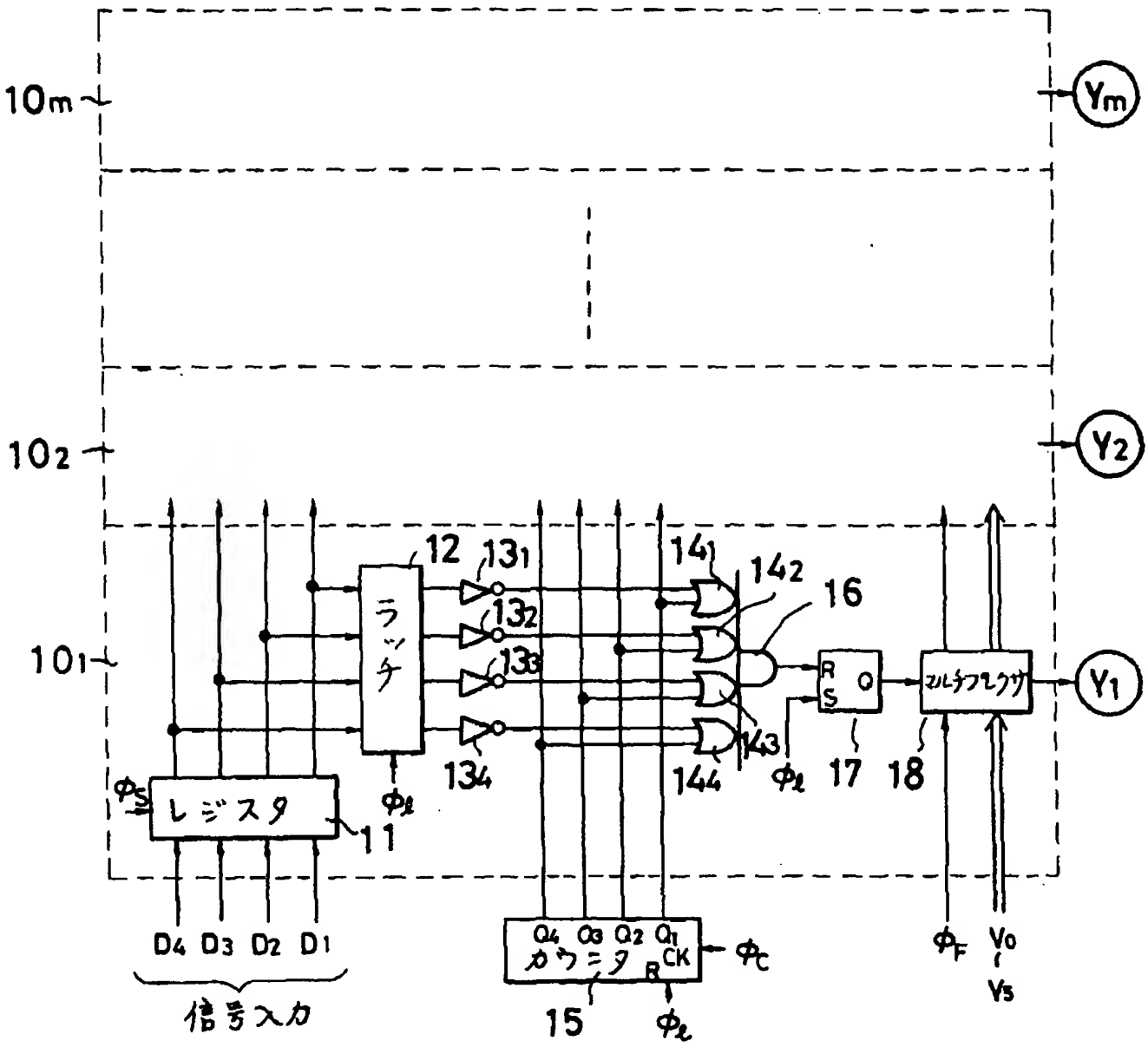
6
7
LC電圧発生回路
V0~V5

[Fig. 4]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14₄
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17
18
ラッチ
レジスタ
11
R
S
Q
マルチプレクサ
φ1
φ2
φ3
φF
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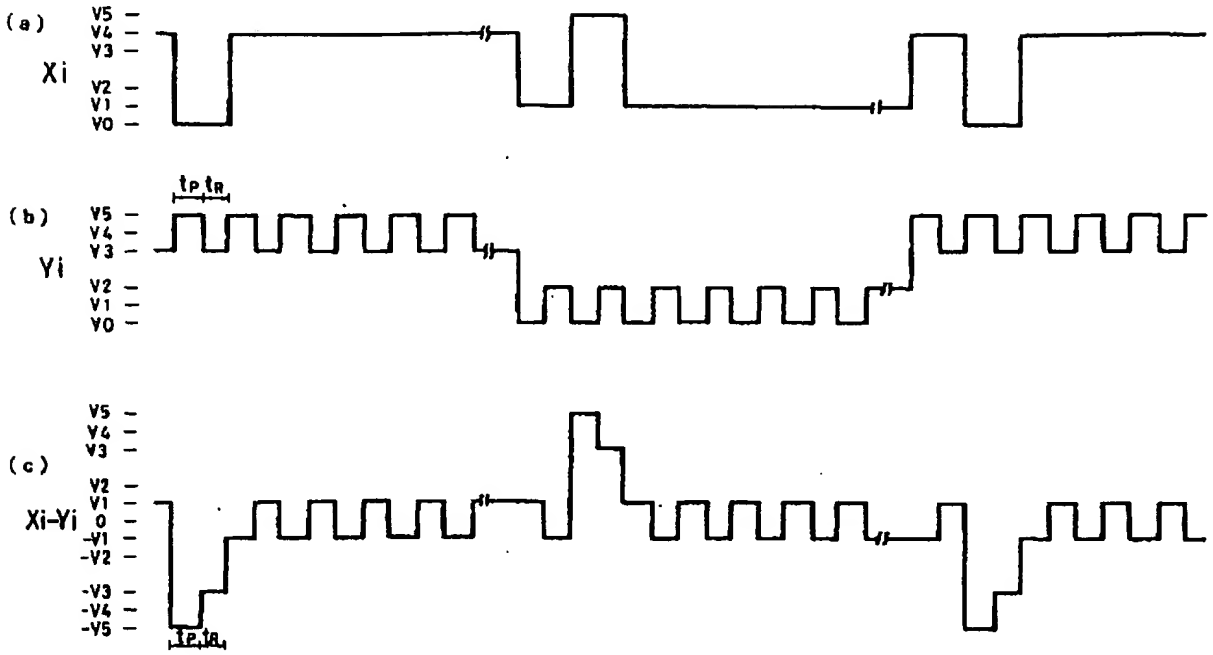
[Fig. 6]



[Translation done.]